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## PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)  
IMPJ-0003D1 (033327-056)

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Signature

Typed or printed

Name Julie Arango

Application Number  
10/661,037

Filed  
09/12/2003

First Named Inventor  
John D. Hyde

Art Unit  
2822

Examiner  
Soward, Ida M.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.  
☐ assignee of record of the entire interest.  
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.  
(Form PTO/SB/96)  
☐ attorney or agent of record.  
Registration number \_\_\_\_\_  
☒ attorney or agent acting under 37 CFR 1.34.  
Registration number 38,745

Signature

Khaled Shami

Typed or printed name

408-292-5800

Telephone number

11/22/2006

Date

☒ \*Total of 1 forms are submitted.

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PATENT  
Serial No. 10/661,037  
Atty. Docket No. IMPJ-0003D1 (033327-056)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: John D. Hyde et al. CONFIRMATION NO.: 6704  
SERIAL NO.: 10/661,037  
FILING DATE: 09/12/2003  
TITLE: pFET SYNAPSE TRANSISTOR WITH STRUCTURE FOR  
FACILITATING CHARGE INJECTION AND/OR TUNNELING WITH  
RESPECT TO A FLOATING GATE  
EXAMINER: Soward, Ida M.  
ART UNIT: 2822

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**CERTIFICATE OF MAILING**

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Julie Arango  
Julie Arango

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Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Sir:

Applicant respectfully requests a formal review of the legal and factual basis of the rejections in the above referenced application in view of the following remarks:

1. The final Office Action fails to account for all the elements recited in the claims. For example, Claim 36 recites first and second n- wells. The final Office Action points to Bergemont's n- well 205 as the second n- well, and to the n- well to the left of that (presumably

203) as the first n- well. However, Claim 36 also recites first and second p+ regions in the first n- well and third and fourth p+ regions in the second n- well. Bergemont shows p+ regions in second n- well 205, but does NOT show any p+ regions in the n- well to the left of that (that is, n- well 203). Bergemont also does not show other claimed features relating to the first n- well (203), such as a channel between a source and a drain, a source contact terminal, and a drain contact terminal. While similar features are shown in relation to the second n- well 205 of Bergemont, none are shown in relation to the first n- well (203) as Claim 36 expressly and clearly recites. Bergemont also fails to teach recited features in other claims, which the Yamashita also fails to teach, and the final Office Action does not address these deficiencies.


2. Bergemont and Yamashita are not properly combinable because their teachings are incompatible. The final Office Action mischaracterizes Applicant's basis for this assertion as advocacy of product-by-process claims. In fact there are no process steps recited in any of Applicant's claims and therefore none of them fall into the class of product-by-process claims. Applicant simply reasoned that the teachings of Bergemont and Yamashita are incompatible because they employ processes that are inconsistent with each other and with their stated goals to achieve products that are also different and incompatible. Bergemont is directed to EEPROM memories, which operate on electron tunneling principals, primarily through gate oxides. Conditions required to permit tunneling are very specific and impose strict limitations on operational, material and dimensional parameters. In addition, the object of Bergemont is to realize a device that can be fabricated consistent with CMOS processing procedures. Otherwise EEPROM devices can only be economically produced in bulk, and cannot be efficiently incorporated into SOC (system-on-chip) devices as Bergemont seeks to do. Yamashita, by

comparison, is not concerned with CMOS processing and introduces numerous fabrication steps that are inconsistent with CMOS processing and would add tremendous costs to the fabrication, in direct contravention of the stated goals of Bergemont. It was this argument against the combination of Bergemont and Yamashita that Applicant advanced and that the final Office Action mischaracterized as an argument for the patentability of product-by-process claims, when in fact no such claims are present in the instant application.

Please charge any additional required fees, or credit any overpayment to our deposit account no. 50-1698.

Respectfully submitted,  
THELEN REID & PRIEST, L.L.P.

Dated: 11/22/2006

  
Khaled Shami  
Reg. No. 38,745

Thelen Reid & Priest LLP  
P.O. Box 640640  
San Jose, CA 95164-0640  
Tel. (408) 282-1855  
Fax. (408) 287-8040